CHEN Shixin 陈时鑫

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EDUCATION

The Chinese University of Hong Kong, Sha Tin, Hong Kong *Aug. 2022 - Jul.2026(Expected)*
Ph.D. in Computer Science and Engineering
Supervisor:Prof. Bei Yu
Research Interest: Hardware Accelerator, Agile IC Design, Chiplet Architecture

Nanjing University, Nanjing, Jiangsu *Sep. 2018 - Jun. 2022*
Bachelor of Engineering in VLSI Design and System Integration, Elite Class, Rank 2/35
Thesis: Design of a DNN Accelerator Based on Winograd Algorithm using Chisel Language

AWARDS

National Scholarship	2019
National Encouragement Scholarship	2020,2021
People's Scholarship	2020,2021,2022
The Yang Lanyun Leadership Scholarship	2021
The Dongliang Special Scholarship	2022
Outstanding Graduate of Jiangsu Province	2022
CUHK Vice-Chancellor's PhD Scholarship	2022
Hong Kong PhD Fellowship Scholarship (HKPFS)	2022

PUBLICATIONS

[C3] **Shixin Chen**, Hengyuan Zhang, Zichao Ling, Jianwang Zhai, Bei Yu, "The Survey of 2.5D Integrated Architecture: An EDA perspective", *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC),* Japan, Jan. 21–23, 2025.

[C2] Mingjun Li*, Pengjia Li*, Shuo Yin, **Shixin Chen**, Beichen Li, Chong Tong, Jianlei Yang, Tinghuan Chen, Bei Yu, "WinoGen: A Highly Configurable Winograd Convolution IP Generator for Efficient CNN Acceleration on FPGA", *ACM/IEEE Design Automation Conference (DAC),*San Francisco, Jun. 23–27, 2024.

[C1] **Shixin Chen**, Su Zheng, Chen Bai, Wenqian Zhao, Shuo Yin, Yang Bai, Bei Yu, "SoC-Tuner: An Importance-guided Exploration Framework for DNN-targeting SoC Design", *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC),* Korea, Jan. 22–25, 2024.

[J2] **Shixin Chen**, Shanyi Li, Zhen Zhuang, Su Zheng, Zheng Liang, Tsung-Yi Ho, Bei Yu, Alberto L. Sangiovanni-Vincentelli, "Floorplet: Performance-aware Floorplan Framework for Chiplet Integration", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).*

[J1] Yang Bai, Xufeng Yao, Qi Sun, Wenqian Zhao, **Shixin Chen**, Zixiao Wang, Bei Yu, "GTCO: Graph and Tensor Co-Design for Transformer-based Image Recognition on Tensor Cores", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).*

EXPERIENCES

SmartMore Co.Ltd *Shenzhen, Guangdong Province*
Research Intern, Heterogeneous Computing Group Jul. 2021 – Sep. 2022
Project: Hardware Accelerator for Super-Resolution Video Based on FPGA

Huawei Noah's Ark Lab *Shenzhen, Guangdong Province*
Research Intern, AI4EDA Group Sept. 2023 – Dec. 2023
Project: Large Language Model for Hardware Verification

iStar Research Group *Shenzhen, Guangdong Province*
Algorithm Researcher, EDA Tool Group Jul. 2024 – Mar. 2025
Project: Matching and Acceleration for Analog Design

RESEARCH

IP-Matcher: An Efficient One-to-Many Analog Circuit IP Matching and Acceleration Framework
Submit to ICCAD 2025 Sept. 2024 - Mar. 2025
Developed tools to improve the matching efficiency and accuracy when reusing the schematic and layout of legacy analog designs. Specialized hashing and acceleration strategies are utilized to prune the matching space to boost analog design efficiency.

CHASE: A CHiplet Architecture Simulation and Exploration Framework with Decoupled Multi-Fidelity Optimization
Submit to ICCAD 2025 Feb. 2024 - Sept. 2024
Developed a simulation and exploration framework for advanced chiplet-based 2.5D architecture with multi-fidelity strategies to improve design efficiency. The simulation framework consists of a toolchain to comprehensively evaluate the chiplet system end-to-end.

An Exploration Framework for RISCV-based SoC for DNN Acceleration
ASP-DAC 2024 Sept. 2022 - Jun. 2023
Developed a framework using Bayesian Optimization to explore the optimal architecture parameters for a RISCV-based SoC that contains host CPU cores, DNN accelerator, RoCC-based Communication.

A Framework for Floorplan and Performance Co-optimization of Chiplet Integration
TCAD 2024 Mar. 2023 - Jun. 2023
Developed performance-aware framework for co-optimizing of the floorplan and performance of chiplet-based architecture. The framework consists of simulation tools for performance reporting and comprehensive cost and reliability optimization models.

Architecture Design of a DNN Accelerator Based on Winograd Algorithm using Chisel Language
Thesis of Bachelor Thesis Jul. 2021 - Mar. 2022
Designed an architecture for Matrix-Multiplication Acceleration based on the Winograd algorithm, which saves multiplication resources to lower hardware cost.

SKILLS

Software Languages	C, C++, Python, Shell
Hardware Languages	Verilog, Chisel, SPICE
Frameworks & Tools	Cadence Virtuoso, Xilinx Vivado, PyTorch, LaTeX, Chipyard, Gem5