Shixin CHEN

Ph.D. Candidate ✿ Department of Computer Science and Engineering
The Chinese University of Hong Kong ✿ Supervisor: Prof. Bei Yu
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EDUCATION

The Chinese University of Hong Kong (CUHK) *Aug. 2022 – Aug. 2026*
Ph.D. in Computer Science and Engineering Hong Kong
Supervisor: Prof. Bei Yu

Nanjing University (NJU) *Sept. 2018 – June 2022*
B.Eng. in VLSI Design and System Integration, Elite Class, Rank 2/35 Nanjing, China

RESEARCH INTERESTS

- Design Space Exploration of Architecture
- 3D/2.5D IC and Chiplet
- Analog Design and Optimization
- Hardware Accelerator
- Machine Learning in EDA

PUBLICATIONS

* represents equal contribution.

Conference Papers

[C8] Yapeng Li, Peng Xu, **Shixin Chen**, Jindong Tu, Tongkai Wu, Chong Tong, Bei Yu, Tinghuan Chen, "AMigration: Analog Placement Migration via Adaptive Constraints Relaxation," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, Nov. 8–12, 2026.

[C7] **Shixin Chen**, Peng Xu, Yapeng Li, Tinghuan Chen, Bei Yu, "PatchWork: A Patch-Driven Framework for Efficient Analog Layout Automation via Legacy Knowledge Reuse," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, California, USA, Nov. 8–12, 2026.

[C6] Zixuan Li*, Kanglin Tian*, Fan Hu, Zirui Li, Xinyue Wu, Hengyuan Zhang, **Shixin Chen**, Jianwang Zhai, Xinfei Guo, Kang Zhao, "ChiPlanner: Physically-Aware and Timing-Driven Design Planner for 2.5D Multi-Chiplet Systems," *ACM/IEEE Design Automation Conference (DAC)*, Long Beach, USA, Jul. 26–29, 2026.

[C5] **Shixin Chen***, Peng Xu*, Yapeng Li, Tinghuan Chen, Bei Yu, "IP-Matcher: An Efficient One-to-Many Matching Framework for Analog Circuit Design and Reusing," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Verona, Italy, Apr. 20–22, 2026.

[C4] **Shixin Chen**, Hengyuan Zhang, Jianwang Zhai, Bei Yu, "CHASE: A CHiplet Architecture Simulation and Exploration Framework with Decoupled Multi-Fidelity Optimization," *ACM International Symposium on Physical Design (ISPD)*, Bonn, Germany, Mar. 15–18, 2026.

[C3] **Shixin Chen**, Hengyuan Zhang, Zichao Ling, Jianwang Zhai, Bei Yu, "The Survey of 2.5D Integrated Architecture: An EDA Perspective," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Japan, Jan. 21–23, 2025. (Invited Paper)

[C2] Mingjun Li*, Pengjia Li*, Shuo Yin, **Shixin Chen**, Beichen Li, Chong Tong, Jianlei Yang, Tinghuan Chen, Bei Yu, "WinoGen: A Highly Configurable Winograd Convolution IP Generator for Efficient CNN Acceleration on FPGA," *ACM/IEEE Design Automation Conference (DAC)*, 2024.

[C1] **Shixin Chen**, Su Zheng, Chen Bai, Wenqian Zhao, Shuo Yin, Yang Bai, Bei Yu, "SoC-Tuner: An Importance-guided Exploration Framework for DNN-targeting SoC Design," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, South Korea, Jan. 22–25, 2024.

Journal Papers

[J3] Peng Xu, Su Zheng, Mingzi Wang, Ziyang Yu, **Shixin Chen**, Tinghuan Chen, Keren Zhu, Tsung-Yi Ho, Bei Yu, "Rank-DSE: Neural Pareto Comparator of Microarchitecture Design Space Exploration," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 30, no. 5, pp. 71:1–71:24, 2025.

[J2] **Shixin Chen**, Shanyi Li, Zhen Zhuang, Su Zheng, Zheng Liang, Tsung-Yi Ho, Bei Yu, Alberto L. Sangiovanni-Vincentelli, "Floorplet: Performance-aware Floorplan Framework for Chiplet Integration," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 43, no. 6, pp. 1638–1649, 2024.

[J1] Yang Bai, Xufeng Yao, Qi Sun, Wenqian Zhao, **Shixin Chen**, Zixiao Wang, Bei Yu, "GTCO: Graph and Tensor Co-Design for Transformer-based Image Recognition on Tensor Cores," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 43, no. 2, pp. 586–599, 2024.

SELECTED AWARDS

Award and Year	**Awarding Institution**
Hong Kong PhD Fellowship Scholarship (HKPFS), 2022	Research Grants Council of Hong Kong
CUHK Vice-Chancellor's PhD Scholarship, 2022	The Chinese University of Hong Kong
Chenxue Overseas Study Scholarship, 2022	Nanjing University
Outstanding Graduate of Jiangsu Province, 2022	The Education Department of Jiangsu Province
The Star of Self-Improvement, 2021	National Union of Students of PRC
The Person of the Year of NJU, 2021	Nanjing University
The Dongliang Special Scholarship, 2021	Nanjing University
National Scholarship, 2019	Education Ministry of PRC
People's Scholarship, 2019–2021	Nanjing University
National Encouragement Scholarship, 2020–2021	Education Ministry of PRC
Student Model of Jiangsu Province, 2020	Jiangsu Province
The Yang Lanyun Leadership Scholarship, 2020	Nanjing University
Electronic Design Competition Second Prize, 2020	Jiangsu Province
Sichuan Chamber of Commerce Scholarship, 2019	Sichuan Chamber of Commerce of Jiangsu Province

EXPERIENCES

SmartMore Co., Ltd. *Jul. 2021 – Sept. 2022*
Research Intern, Heterogeneous Computing Group Shenzhen, Guangdong Province
Topic: Hardware Accelerator for Super-resolution Video

Huawei Noah's Ark Lab *Sept. 2023 – Dec. 2023*
Research Intern, AI4EDA Group Shenzhen, Guangdong Province
Topic: Large Language Model for Hardware Verification

ACADEMIC SERVICE

Conference Reviewer

- ACM International Symposium on Physical Design (ISPD), 2024

- ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2025

Journal Reviewer

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)

SKILLS

Software Languages	C, C++, Python, Bash
Hardware Languages	SystemVerilog, Chisel
Tools	Xilinx Vivado, PyTorch, LaTeX
Frameworks	Chipyard, Gem5
Hobbies	Guitar, Chinese Calligraphy, Badminton

TEACHING

- CSCI2010, Fall 2023, Digital Logic Design Laboratory
- CSCI3420, Spring 2023, Computer Organization and Design
- CSCI3420, Spring 2024, Computer Organization and Design